AMENDMENTS TO THE CLAIMS

1. (Original) A semiconductor device comprising:

a die having:

a semiconductor substrate;

a plurality of device conductive regions formed in and over the substrate; and

an interconnect structure formed on the substrate to make electrical connections with the device conductive regions, and form a top surface of the die, the interconnect structure including:

a dielectric structure that contacts the substrate; and

a plurality of layers of metal that are formed in and isolated by the dielectric structure, each metal layer having a plurality of metal traces; and

a conductive region formed over the top surface of the die above the plurality of layers of metal.

2. (Original) The semiconductor device of claim 1 wherein the conductive region includes silicon.

3. (Original) The semiconductor device of claim 2 wherein the silicon is attached via an adhesive.

4. (Original) The semiconductor device of claim 2 and further comprising:

a first via that makes an electrical connection with a region of a metal trace and a first end of the conductive region; and

a second via that makes an electrical connection with a region of a metal trace and a second end of the conductive region.

5. (Original) The semiconductor device of claim 2 wherein the conductive region has a concentration of dopant atoms.

6. (Original) The semiconductor device of claim 2 and further comprising:

a dielectric region formed to contact the conductive region; and

a conductor region formed to contact the dielectric region.

7. (Original) The semiconductor device of claim 6 and further comprising:

a first via that makes an electrical connection with a region of a metal trace and the conductive region; and

a second via that makes an electrical connection with a region of a metal trace and the conductor region.

8. (Original) The semiconductor device of claim 7 wherein the conductive region has a concentration of dopant atoms.

9. (Original) The semiconductor device of claim 2 wherein the dielectric structure includes a plurality of layers, including an overlying passivation layer, the conductive region being formed over the passivation layer.

10. (Original) The semiconductor device of claim 9 and further comprising:

a plurality of contacts formed in the dielectric structure, the contacts electrically connecting the device conductive regions to the metal traces that are formed from a first layer of metal;

a plurality of vias formed in the dielectric structure, the vias electrically connecting vertically adjacent metal traces and regions; and

a plurality of pads formed in the dielectric structure, the pads being connected to a number of vias to form external points of electrical connection.

Claims 11-18 (Cancelled).

19. (Original) The semiconductor device of claim 1 wherein the conductive region is non-metallic.

20. (Original) The semiconductor device of claim 19 wherein the conductive region has a concentration of dopant atoms.

21. (New) A semiconductor device comprising:

a die having:

a semiconductor substrate;

a plurality of conductive regions formed in and near the substrate; and

an interconnect structure having a nonconductive top surface, and a bottom surface that contacts the substrate, the interconnect structure having:

a dielectric structure,

a plurality of metal interconnects formed within the dielectric structure, the metal interconnects making electrical connections with the plurality of conductive regions, and

a plurality of pads that contact the top surface, the plurality of pads being electrically connected to the conductive regions via the metal interconnects.

22. (New) The semiconductor device of claim 21 and further comprising:

a test structure that contacts the top surface;

a first opening formed in the dielectric structure, the first opening extending from the top surface down to a first region on a metal interconnect; and

a first conductive structure formed in the first opening to make an electrical contact with the first region, and on the top surface to make an electrical connection with the test structure.

23. (New) The semiconductor device of claim 22 wherein the test structure is a capacitor.

24. (New) The semiconductor device of claim 22 wherein the test structure is a resistor.

25. (New) The semiconductor device of claim 22 and further comprising:

a second opening formed in the dielectric structure, the second opening extending from the top surface down to a second region on the metal interconnect; and

a second conductive structure formed in the second opening to make an electrical contact with the second region, and on the top surface to make an electrical connection with the test structure.

26. (New) The semiconductor device of claim 25 wherein the test structure is a capacitor.

27. (New) The semiconductor device of claim 25 wherein the test structure is a resistor.

28. (New) The semiconductor device of claim 25 and further comprising a third opening formed in the dielectric structure, the third opening extending through the metal interconnect to break an electrical connection between the first and second regions of the metal interconnect.